ispLSI® and pLSI® 2032

High Density Programmable Logic

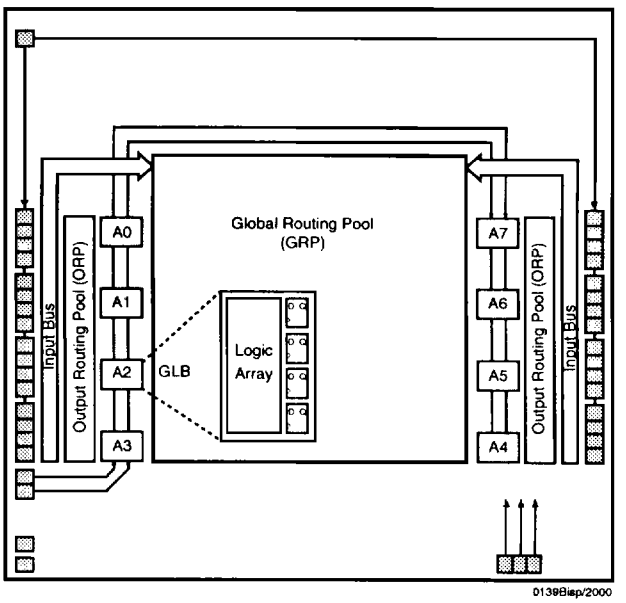
Features

- **HIGH DENSITY PROGRAMMABLE LOGIC**
  - **1000 PLD Gates**
  - **32 I/O Pins, Two Dedicated Inputs**
  - **32 Registers**
  - **High Speed Global Interconnect**
  - **Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **Small Logic Block Size for Random Logic**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **f_{max} = 154 MHz Maximum Operating Frequency**
  - **t_{pd} = 5.5 ns Propagation Delay**
  - **TTL Compatible Inputs and Outputs**
  - **Electrically Erasable and Reprogrammable**
  - **Non-Volatile**
  - **100% Tested at Time of Manufacture**
  - **Unused Product Term Shutdown Saves Power**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **In-System Programmable 5-Volt Only**
  - **Change Logic and Interconnects "On-the-Fly" in Seconds**
  - **Reprogram Soldered Devices for Debugging**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **Three Dedicated Clock Input Pins**
  - **Synchronous and Asynchronous Clocks**
  - **Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **Flexible Pin Placement**
  - **Optimized Global Routing Pool Provides Global Interconnectivity**
- **pLSI/ispLSI DEVELOPMENT SYSTEM (pDS®)**

  pDS Software
  - **Easy to Use PC Windows™ Interface**
  - **Boolean Logic Compiler**
  - **Manual Partitioning**
  - **Automatic Place and Route**
  - **Static Timing Table**

  pDS+™ Software
  - **Industry Standard, Third Party Design Environments**
  - **Schematic Capture, State Machine, HDL**
  - **Automatic Partitioning and Place and Route**
  - **Comprehensive Logic and Timing Simulation**
  - **PC and Workstation Platforms**

Functional Block Diagram



Description

The Lattice ispLSI and pLSI 2032 are High Density Programmable Logic Devices. The devices contain 32 Registers, 32 Universal I/O pins, two Dedicated Input Pins, three Dedicated Clock Input Pins, one dedicated Global OE input pin and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2032 features 5-Volt in-system programmability and in-system diagnostic capabilities. The ispLSI 2032 offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 2032 device, but multiplexes four input pins to control in-system programming.

The basic unit of logic on the ispLSI and pLSI 2032 devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. A7 (see figure 1). There are a total of eight GLBs in the ispLSI and pLSI 2032 devices. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

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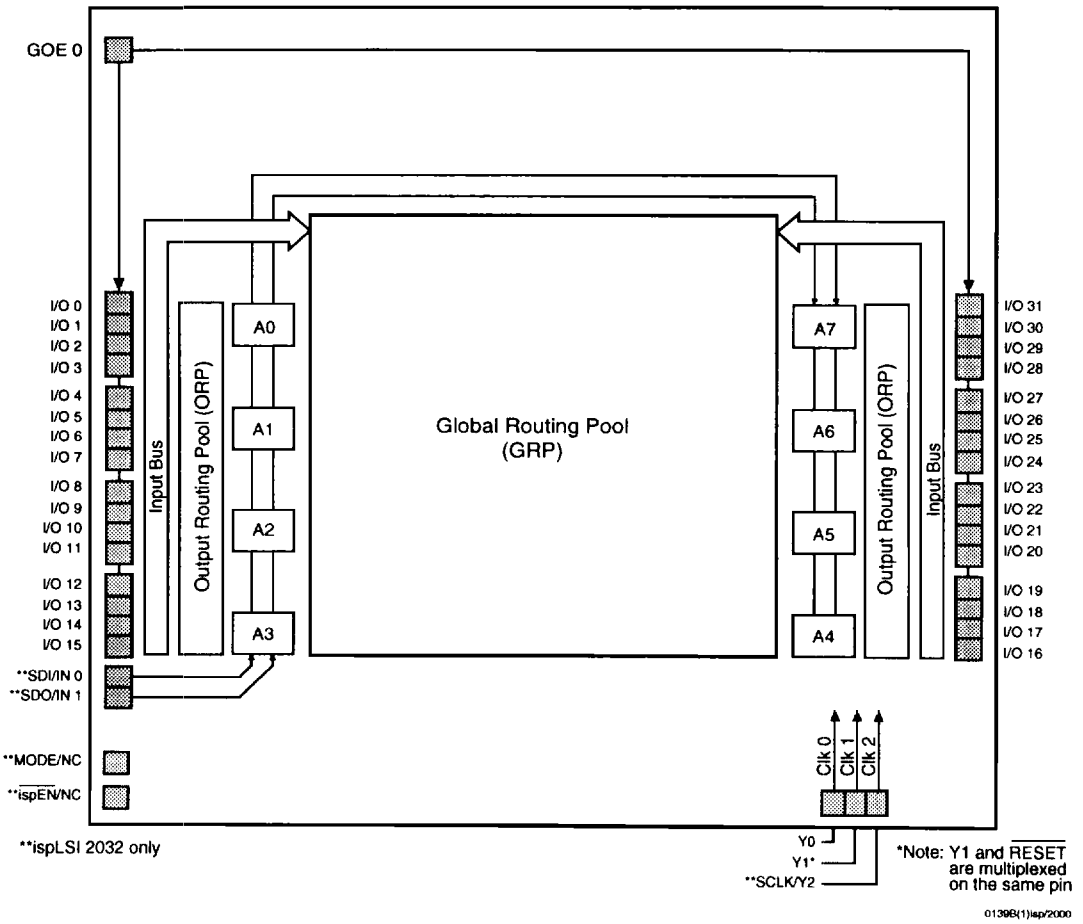
Order #: DS0060

Functional Block Diagram

Figure 1. ispLSI and pLSI 2032 Functional Block Diagram



The devices also have 32 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 32 I/O cells, two dedicated inputs and two ORPs are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 32 universal I/O cells by the ORP. Each ispLSI and pLSI 2032 device contains one Megablock.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI and pLSI 2032 devices are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Ambient Temp. with Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	70	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC} +1	V

Table 2 - 0005/2032

Capacitance (T_A=25°C,f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	8	pf	V_{CC} = 5.0V, V_{IN} = 2.0V
C_2	I/O and Clock Capacitance	10	pf	V_{CC} = 5.0V, $V_{I/O}$, V_Y = 2.0V

Table 2 - 0006

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	1000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2 - 0008A-2032-isp

Switching Test Conditions

Input Pulse Levels	GND to 3.0V	
Input Rise and Fall Time 10% to 90%	-150	≤ 1.5 ns
	-135	≤ 2 ns
	Others	≤ 3 ns
Input Timing Reference Levels	1.5V	
Ouput Timing Reference Levels	1.5V	
Output Load	See figure 2	

Table 2 - 0003/2032

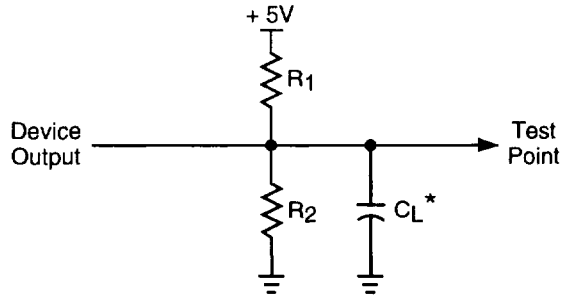
3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} -0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} -0.5V	470Ω	390Ω	5pF

Table 2 - 0004A

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}		–	–	10	µA
$I_{IL\text{-}isp}$	$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
$I_{IL\text{-}PU}$	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V		-45	–	-200	mA
I_{CC}[2]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V f_{TOGGLE} = 1 MHz	-150	–	60	150	mA
			Others	–	60	120	mA

Table 2 - 0007Aisp/2032

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using two 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[4] COND.	#[2]	DESCRIPTION[1]	-150		-135		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	5.5	–	7.5	ns
t_{pd2}	A	2	Data Propagation Delay	–	8.0	–	10.0	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[3]	154	–	137	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	111	–	100	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle	167	–	167	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	3.0	–	4.0	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	4.5	–	4.5	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	4.5	–	5.5	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	5.0	–	5.5	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	8.0	–	10.0	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	4.5	–	5.0	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	11.0	–	12.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	11.0	–	12.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	5.0	–	6.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	5.0	–	6.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	3.0	–	3.0	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	3.0	–	3.0	–	ns

Table 2 - 0030B/2032-150

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions Section.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[4] COND.	#[2]	DESCRIPTION[1]	-110		-80		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	10.0	–	15.0	ns
t_{pd2}	A	2	Data Propagation Delay	–	13.0	–	18.5	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[3]	111	–	84	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $(\frac{1}{t_{su2} + t_{co1}})$	77	–	57	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle	125	–	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	5.5	–	7.5	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	5.5	–	8.0	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	7.5	–	9.5	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	6.5	–	9.5	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	13.5	–	19.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	6.5	–	10.0	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	14.5	–	24.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	14.5	–	24.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	7.0	–	12.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	7.0	–	12.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	4.0	–	6.0	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	4.0	–	6.0	–	ns

Table 2 - 0030B/2128-110

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-150		-135		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{io}	20	Input Buffer Delay	–	0.6	–	1.1	ns
t_{din}	21	Dedicated Input Delay	–	1.1	–	2.2	ns
GRP							
t_{grp}	22	GRP Delay	–	0.7	–	1.3	ns
GLB							
t_{4ptbpc}	23	4 Product Term Bypass Path Delay (Combinatorial)	–	2.6	–	3.6	ns
t_{4ptbpr}	24	4 Product Term Bypass Path Delay (Registered)	–	3.1	–	3.6	ns
t_{1ptxor}	25	1 Product Term/XOR Path Delay	–	4.3	–	5.0	ns
$t_{20ptxor}$	26	20 Product Term/XOR Path Delay	–	4.6	–	5.1	ns
t_{xoradj}	27	XOR Adjacent Path Delay[3]	–	5.0	–	5.6	ns
t_{gbp}	28	GLB Register Bypass Delay	–	0.0	–	0.0	ns
t_{gsu}	29	GLB Register Setup Time befor Clock	0.7	–	0.3	–	ns
t_{gh}	30	GLB Register Hold Time after Clock	1.8	–	3.0	–	ns
t_{gco}	31	GLB Register Clock to Output Delay	–	0.8	–	0.7	ns
t_{gro}	32	GLB Register Reset to Output Delay	–	1.2	–	1.1	ns
t_{ptre}	33	GLB Product Term Reset to Register Delay	–	2.9	–	4.4	ns
t_{ptoe}	34	GLB Product Term Output Enable to I/O Cell Delay	–	6.9	–	6.4	ns
t_{ptck}	35	GLB Product Term Clock Delay	2.5	4.1	2.9	5.2	ns
ORP							
t_{orp}	36	ORP Delay	–	0.8	–	1.3	ns
t_{orpbp}	37	ORP Bypass Delay	–	0.3	–	0.3	ns
Outputs							
t_{ob}	38	Output Buffer Delay	–	1.3	–	1.2	ns
t_{obs}	39	Output Buffer Delay, Slew Limited	–	11.3	–	11.2	ns
t_{oen}	40	I/O Cell OE to Output Enabled	–	2.8	–	3.2	ns
t_{odis}	41	I/O Cell OE to Output Disabled	–	2.8	–	3.2	ns
t_{goe}	42	Global Output Enable	–	2.2	–	2.8	ns
Clocks							
t_{gy0}	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	2.1	2.1	2.3	2.3	ns
$t_{gy1/2}$	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.1	2.1	2.3	2.3	ns
Global Reset							
t_{gr}	45	Global Reset to GLB	–	4.7	–	6.4	ns

Table 2- 0036C/2032-150

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

External Timing Parameters

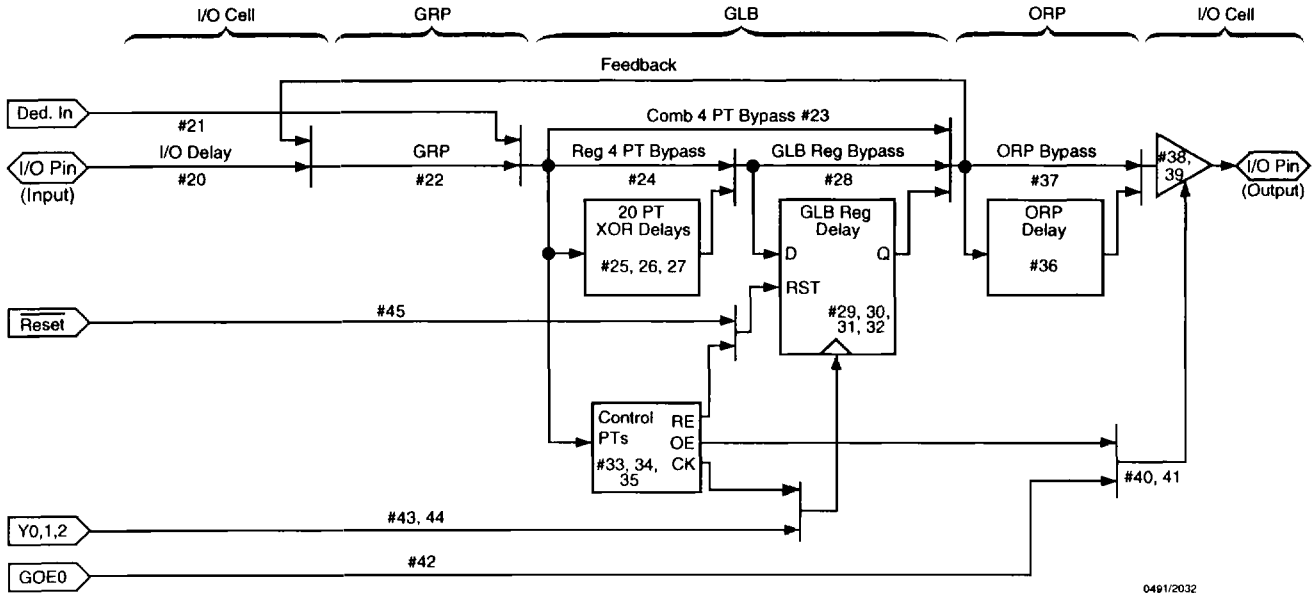
Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-110		-80		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{io}	20	Input Buffer Delay	–	1.7	–	2.2	ns
t_{din}	21	Dedicated Input Delay	–	3.1	–	4.6	ns
GRP							
t_{grp}	22	GRP Delay	–	1.7	–	2.6	ns
GLB							
t_{4ptbpc}	23	4 Product Term Bypass Path Delay (Combinatorial)	–	4.9	–	7.2	ns
t_{4ptbpr}	24	4 Product Term Bypass Path Delay (Registered)	–	4.8	–	7.2	ns
t_{1ptxor}	25	1 Product Term/XOR Path Delay	–	6.2	–	8.8	ns
$t_{20ptxor}$	26	20 Product Term/XOR Path Delay	–	6.8	–	9.2	ns
t_{xoradj}	27	XOR Adjacent Path Delay[3]	–	7.5	–	10.2	ns
t_{gbp}	28	GLB Register Bypass Delay	–	0.1	–	0.0	ns
t_{gsu}	29	GLB Register Setup Time befor Clock	0.5	–	0.1	–	ns
t_{gh}	30	GLB Register Hold Time after Clock	4.0	–	6.0	–	ns
t_{gco}	31	GLB Register Clock to Output Delay	–	0.6	–	0.4	ns
t_{gro}	32	GLB Register Reset to Output Delay	–	1.8	–	2.2	ns
t_{ptre}	33	GLB Product Term Reset to Register Delay	–	5.9	–	8.8	ns
t_{ptoe}	34	GLB Product Term Output Enable to I/O Cell Delay	–	7.1	–	12.8	ns
t_{ptck}	35	GLB Product Term Clock Delay	4.0	7.0	5.5	9.5	ns
ORP							
t_{orp}	36	ORP Delay	–	1.5	–	2.1	ns
t_{orpbp}	37	ORP Bypass Delay	–	0.5	–	0.6	ns
Outputs							
t_{ob}	38	Output Buffer Delay	–	1.2	–	2.4	ns
t_{obs}	39	Output Buffer Delay, Slew Limited	–	11.2	–	12.4	ns
t_{oen}	40	I/O Cell OE to Output Enabled	–	4.0	–	6.4	ns
t_{odis}	41	I/O Cell OE to Output Disabled	–	4.0	–	6.4	ns
t_{goe}	42	Global Output Enable	–	3.0	–	5.6	ns
Clocks							
t_{gy0}	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	3.2	3.2	4.6	4.6	ns
$t_{gy1/2}$	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	3.2	3.2	4.6	4.6	ns
Global Reset							
t_{gr}	45	Global Reset to GLB	–	9.0	–	12.8	ns

Table 2- 0036C/2032-110

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

ispLSI and pLSI 2032 Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu	=	Logic + Reg su - Clock (min)
	=	(tio + tgrp + t20ptxor) + (tgsu) - (tio + tgrp + tptck(min))
	=	(#20+ #22+ #26) + (#29) - (#20+ #22+ #35)
1.9 ns	=	(1.1 + 1.3 + 5.1) + (0.3) - (1.1 + 1.3 + 2.9)
th	=	Clock (max) + Reg h - Logic
	=	(tio + tgrp + tptck(max)) + (tgh) - (tio + tgrp + t20ptxor)
	=	(#20+ #22+ #35) + (#30) - (#20+ #22+ #26)
1.4 ns	=	(1.1 + 1.3 + 5.2) + (3.0) - (1.1 + 1.3 + 5.1)
tco	=	Clock (max) + Reg co + Output
	=	(tio + tgrp + tptck(max)) + (tgco) + (torp + tob)
	=	(#20+ #22+ #35) + (#31) + (#36 + #38)
9.1 ns	=	(1.1 + 1.3 + 5.2) + (0.7) + (1.3 + 1.2)

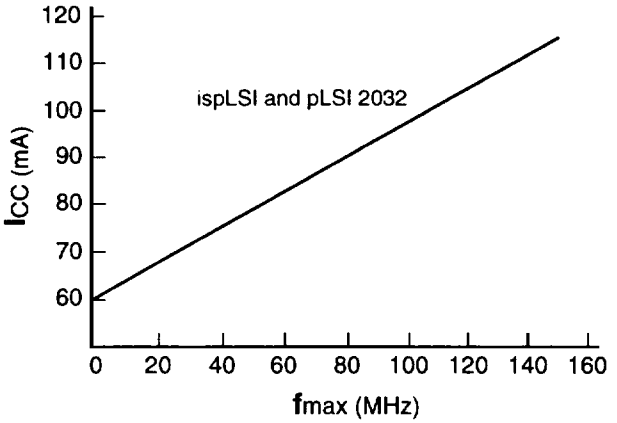
Table 2- 0042-16/2032

Note: Calculations are based upon timing specifications for the ispLSI and pLSI 2032-135L.

Power Consumption

Power Consumption in the ispLSI and pLSI 2032 device depends on two primary factors: the speed at which the device is operating and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of Two 16-bit Counters
Typical Current at 5V, 25° C

I_{CC} can be estimated for the ispLSI and pLSI 2032 using the following equation:

I_{CC} = 23 + (# of PTs * 0.33) + (# of nets * Max freq * 0.011) where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

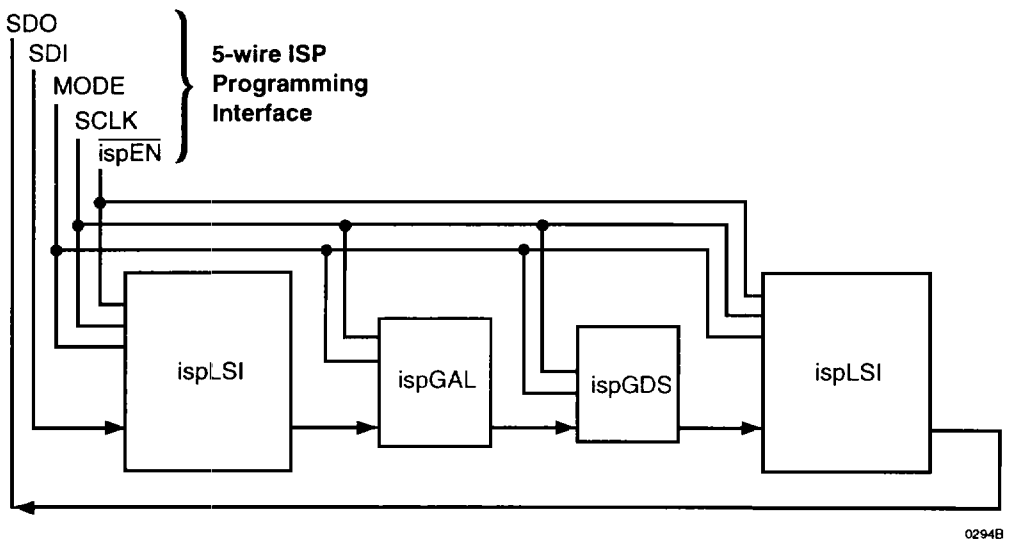
0127A-16-80-isp/2000

In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice high density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The simple signals for interface include isp Enable (ispEN), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme of the programming interface for the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to Lattice's In-System Programmability Manual.

Figure 4. ISP Programming Interface



ISP Programming Voltage/Timing Specifications

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CCP}	Programming Voltage		4.75	5.0	5.25	V
I_{CCP}	Programming Supply Current		–	50	100	mA
V_{IHP}	Input Voltage High	$\overline{ispEN}$ = Low	2.0	–	V_{CCP}	V
V_{ILP}	Input Voltage Low		0.0	–	0.8	V
I_{IP}	Input Current		–	100	200	µA
V_{OHP}	Output Voltage High	I_{OH} = -3.2 mA	2.4	–	V_{CCP}	V
V_{OLP}	Output Voltage Low	I_{OL} = 5 mA	0.0	–	0.5	V
t_r, t_f	Input Rise and Fall		–	–	0.1	µs
t_{ispen}	$\overline{ispEN}$ to Output 3-State Enabled		–	–	10	µs
t_{ispdis}	$\overline{ispEN}$ to Output 3-State Disabled		–	–	10	µs
t_{su}	Setup Time		0.1	–	–	µs
t_{co}	Clock to Output		–	–	0.1	µs
t_h	Hold Time		0.1	–	–	µs
t_{clkh}, t_{clkl}	Clock Pulse Width, High and Low		0.5	–	–	µs
t_{pwv}	Verify Pulse Width		20	–	–	µs
t_{pwp}	Programming Pulse Width		80	–	160	ms
t_{bew}	Bulk Erase Pulse Width		200	–	–	ms
t_{rst}	Reset Time from Valid V_{CCP}	Rise Time < 50 µs	45	–	–	µs

Table 2 - 0029isp-2032

Figure 5. Timing Waveform for ISP Operation

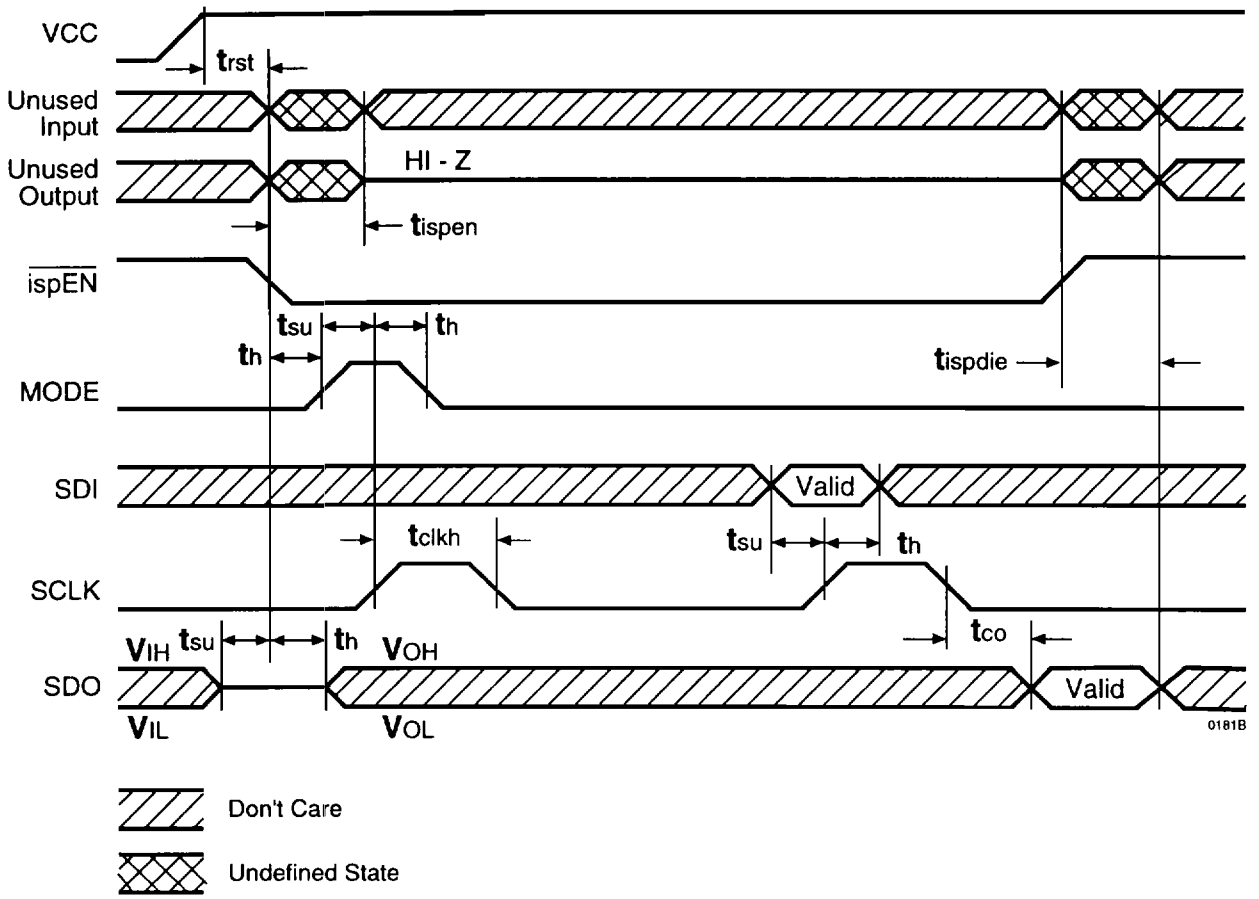


Figure 6. Program, Verify & Bulk Erase Waveform

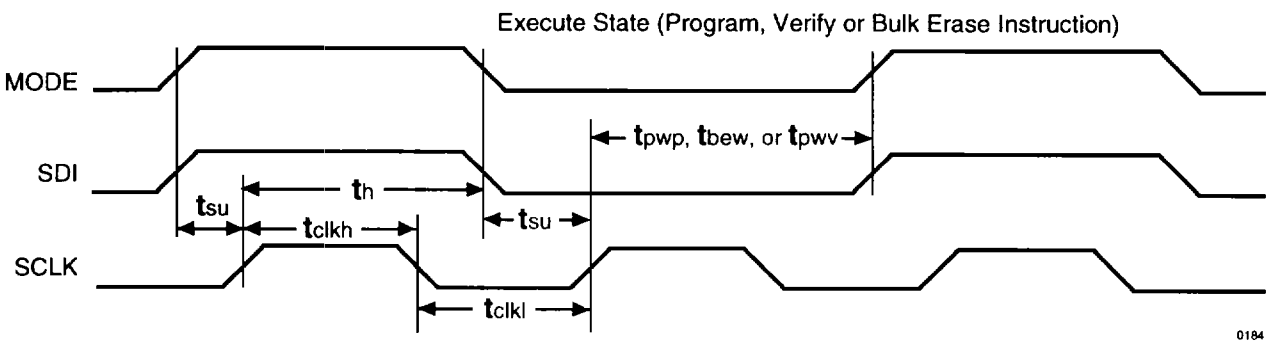
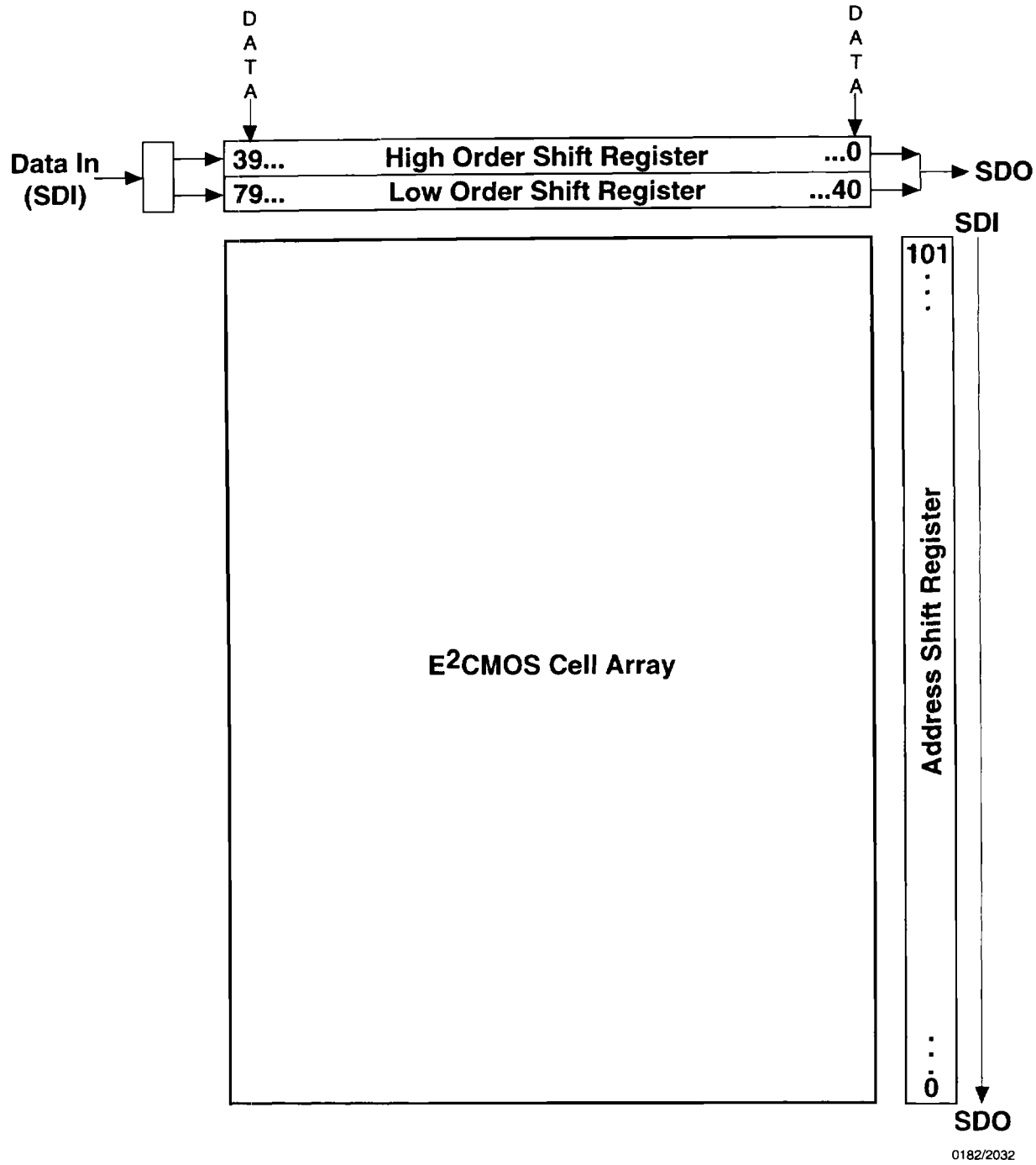


Figure 7. ispLSI 2032 Shift Register Layout



Note: A logic "1" in the address shift register enables the row for programming or verification. A logic "0" disables it.

Pin Description

NAME	PLCC PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31	15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 28, 29, 30, 31, 32, 37, 38, 39, 40, 41, 42, 43, 44, 3, 4, 5, 6, 7, 8, 9, 10	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE 0	2	Global Output Enable input pin.
Y0	11	Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs on the device.
Y1/$\overline{\text{RESET}}$	35	This pin performs two functions: - Dedicated clock input. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. - Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
$\overline{\text{ispEN}}$**/NC	13	Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI*/IN0	14	Input - This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN0 also is used as one of the two control pins for the isp state machine.
MODE*/NC	36	Input - When in ISP Mode, controls operation of ISP state-machine.
SDO*/IN1	24	Input/Output - This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.
SCLK*/Y2	33	Input - This pin performs two functions. It is a dedicated clock input when $\overline{\text{ispEN}}$ is logic high. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
GND	1, 23	Ground (GND)
VCC	12, 34	V_{CC}

Table 2 - 0002A-08isp/2000

* ispLSI 2032 only

** $\overline{\text{ispEN}}$ for ispLSI 2032 only, NC for pLSI 2032 must be left floating or tied to V_{CC}, must not be grounded or tied to any other signal.

Pin Description

NAME	TQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31	9, 10, 11, 12, 13, 14, 15, 16, 19, 20, 21, 22, 23, 24, 25, 26, 31, 32, 33, 34, 35, 36, 37, 38, 41, 42, 43, 44, 1, 2, 3, 4	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE 0	40	Global Output Enable input pin.
Y0	5	Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs on the device.
Y1/$\overline{\text{RESET}}$	29	This pin performs two functions: - Dedicated clock input. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. - Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
$\overline{\text{ispEN}}$**/NC	7	Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI*/IN0	8	Input - This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN0 also is used as one of the two control pins for the isp state machine.
MODE*/NC	30	Input - When in ISP Mode, controls operation of ISP state-machine.
SDO*/IN1	18	Input/Output - This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.
SCLK*/Y2	27	Input - This pin performs two functions. It is a dedicated clock input when $\overline{\text{ispEN}}$ is logic high. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
GND	17, 39	Ground (GND)
VCC	6, 28	V_{CC}

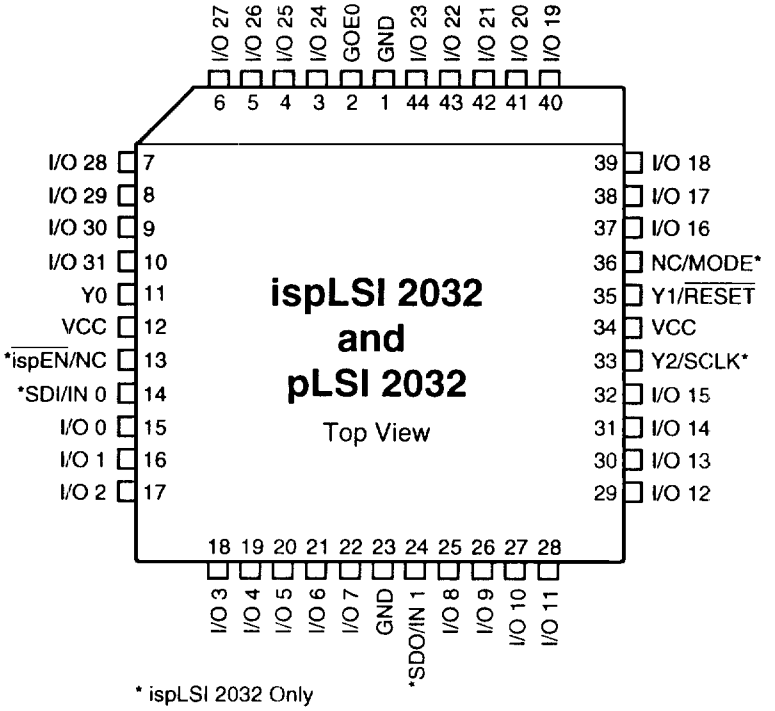
Table 2 - 0002B-2032

* ispLSI 2032 only

** $\overline{\text{ispEN}}$ for ispLSI 2032 only, NC for pLSI 2032 must be left floating or tied to V_{CC}, must not be grounded or tied to any other signal.

Pin Configuration

ispLSI and pLSI 2032 44-pin PLCC

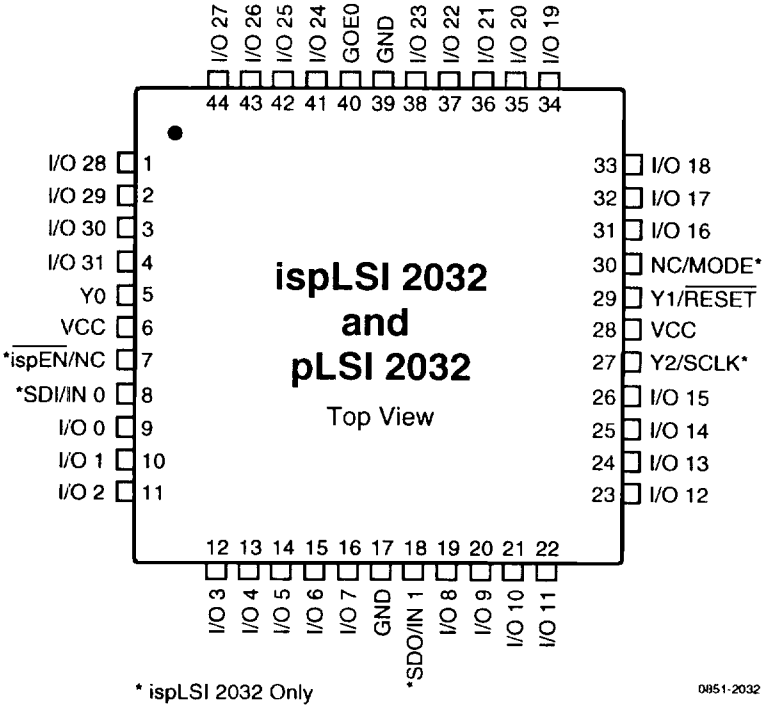


* ispLSI 2032 Only

0123B3/2000

Pin Configuration

ispLSI and pLSI 2032 44-pin TQFP



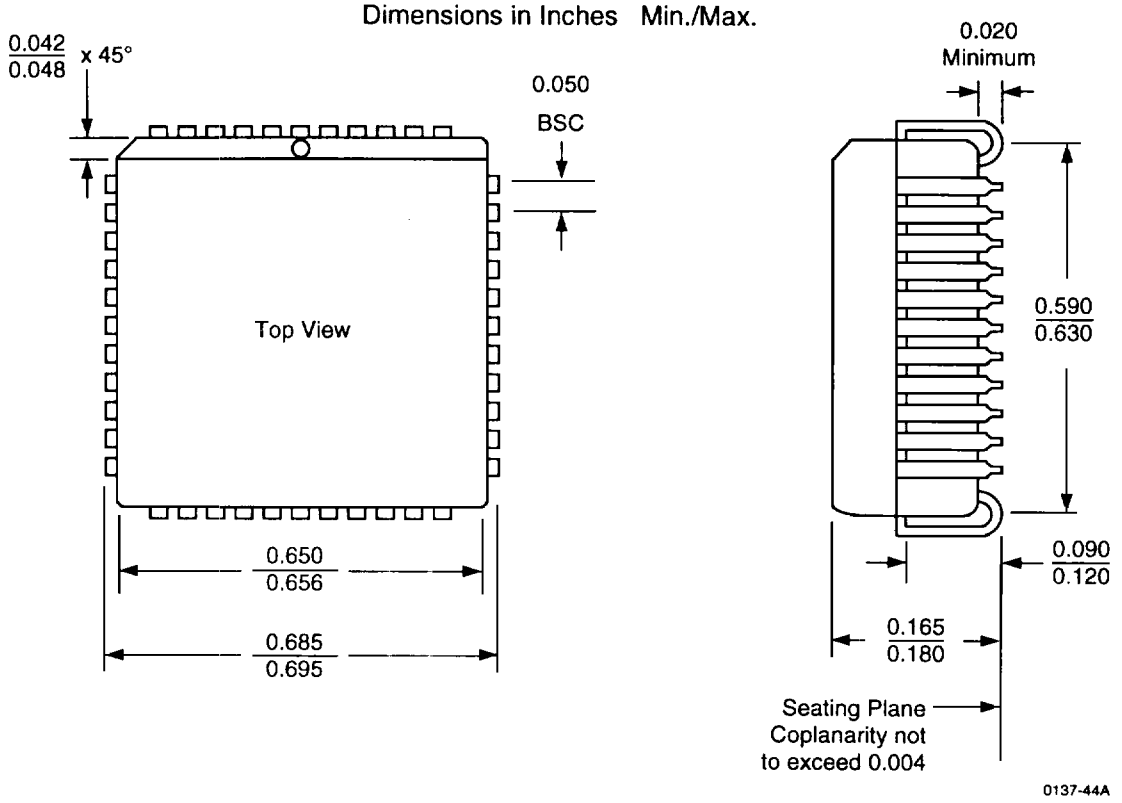
* ispLSI 2032 Only

0851-2032

Package Diagram

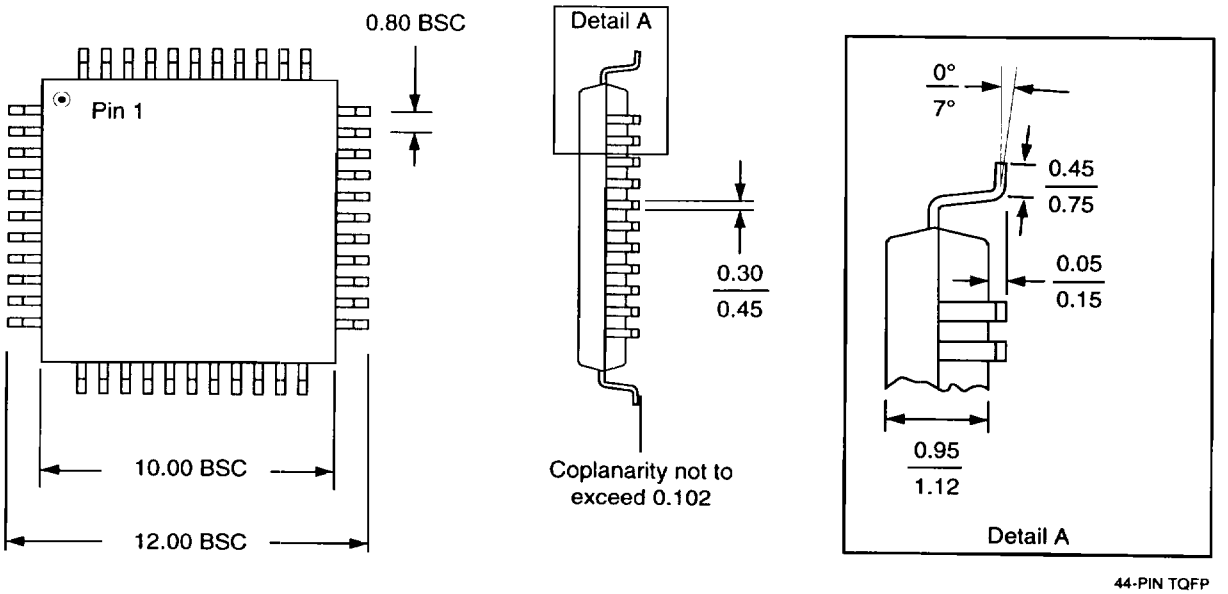
44-Pin PLCC Package

Dimensions in Inches Min./Max.

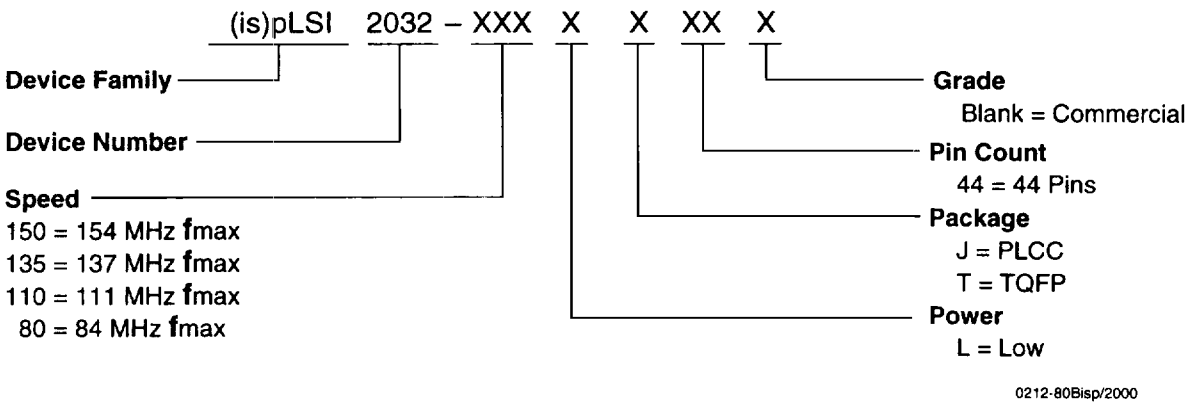


44-Pin TQFP Package

Dimensions in Millimeters Min./Max.



Part Number Description



ispLSI and pLSI 2032 Ordering Information

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	154	5.5	ispLSI 2032-150LJ44	44-Pin PLCC
	137	7.5	ispLSI 2032-135LJ44	44-Pin PLCC
	137	7.5	ispLSI 2032-135LT44	44-Pin TQFP
	111	10	ispLSI 2032-110LJ44	44-Pin PLCC
	111	10	ispLSI 2032-110LT44	44-Pin TQFP
	84	15	ispLSI 2032-80LJ44	44-Pin PLCC
	84	15	ispLSI 2032-80LT44	44-Pin TQFP
pLSI	154	5.5	pLSI 2032-150LJ44	44-Pin PLCC
	137	7.5	pLSI 2032-135LJ44	44-Pin PLCC
	137	7.5	pLSI 2032-135LT44	44-Pin TQFP
	111	10	pLSI 2032-110LJ44	44-Pin PLCC
	111	10	pLSI 2032-110LT44	44-Pin TQFP
	84	15	pLSI 2032-80LJ44	44-Pin PLCC
	84	15	pLSI 2032-80LT44	44-Pin TQFP

Table 2- 0041A-08isp/2000